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EXAMINER	
DOTY, HEATHER ANNE	

ART UNIT	PAPER NUMBER
2813	

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Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

Office Action Summary	Application No.	Applicant(s)	
	10/718,892	JAWARANI ET AL.	
	Examiner	**Art Unit**	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,7-14,17-28,30,31,34-36 and 42-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-14,17-28,30,31,34-36 and 42-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 34 is objected to because of the following informalities: claim 34 recites the limitation "the silicon substrate" in line 4. There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 7, 9, 19, 21, 23, 24, 26, 36, 44, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi et al. (U.S. 5,475,244) in view of Kluth et al. (U.S. 6,486,062), considered with Murakoshi (U.S. 5,770,512) for a showing of inherency for claims 3, 36, and 45.

Regarding claim 1, Koizumi et al. teaches a method of forming a contact to a source/drain contact region of a transistor device having a gate, and the source/drain contact region is comprised substantially of silicon, the method comprising:

- Implanting germanium into a region of the source/drain contact region using the gate as a mask (Fig. 27B; column 11, lines 34-50);
- Activating the germanium implanted into the source/drain contact region (column 11, lines 34-50); and

- Implanting a source/drain dopant into the source/drain contact, wherein the implanting the source/drain dopant is performed subsequent to the activating the germanium (column 11, lines 51-52).

Koizumi et al. does not teach implanting the germanium at a dose not exceeding 1E17-cm^2, or forming a nickel silicide over the source/drain contact region after the activating to form the contact.

Koizumi et al. does teach implanting the germanium at a dose of 4E17 atoms per centimeter, and it has been held that "where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller* 105 USPQ233, 255 (CCPA 1955)."

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Koizumi et al. and optimize the conditions to arrive at a germanium implantation dose of not more than 1E17/cm^2.

Kluth et al. teaches a method of forming source/drain contacts including forming a nickel silicide over the source/drain contact region (column 4, lines 36-38).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a semiconductor device according to the method taught by Koizumi et al. and forming a nickel silicide, as taught by Kluth et al. The motivation for doing so at the time of the invention would have been to produce a silicide that forms a first low-resistivity phase at relatively low temperatures (column 2, lines 15-20) to decrease the resistance of the source/drain contacts.

Regarding claim 2, Koizumi et al. and Kluth et al. together teach the method of claim 1. Koizumi et al. further teaches that activating the atoms further includes activating the atoms in order to make the atoms substitutional in a lattice of the source/drain region, wherein the lattice includes atoms of the first material (column 11, lines 64-66).

Regarding claim 3, Koizumi et al. and Kluth et al. together teach the method of claim 1. Koizumi et al. further teaches that activating the atoms increases a lattice constant of the lattice in the source/drain contact region (Si has lattice constant 0.543 nm, Ge has lattice constant 0.566 nm, SiGe has lattice constant between 0.543 and 0.566 nm, depending upon the Ge concentration, see U.S. 5,770,512 to Murakoshi et al.).

Regarding claims 7 and 9, Koizumi et al. and Kluth et al. together teach the method of claim 1. Koizumi et al. further teaches that the activating includes heating the source/drain contact region to a temperature greater than 550 C and in a range of approximately 900-1400 C (column 11, lines 45-50).

Regarding claim 19, Koizumi et al. and Kluth et al. together teach the method of claim 1. Koizumi et al. further teaches that the gate is over a semiconductor substrate, the source/drain contact region is in the semiconductor substrate, and the source/drain contact region is disposed laterally from the gate (Fig. 27B).

Regarding claim 21, Koizumi et al. and Kluth et al. together teach the method of claim 19. Koizumi et al. further teaches implanting the germanium with an energy of at least 3 keV (500 KeV—column 11, lines 43-44).

Regarding claim 23, Koizumi et al. and Kluth et al. together teach the method of claim 19. Koizumi et al. further teaches implanting the germanium at a dose of at least 1E13/cm^2 (column 11, line 44).

Regarding claim 24, Koizumi et al. and Kluth et al. together teach the method of claim 19. Koizumi et al. further teaches implanting the germanium at a dose of 4E17/cm^2. However, it has been held that "where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller* 105 USPQ233, 255 (CCPA 1955)."

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Koizumi et al. and optimize the conditions to arrive at a germanium implantation dose between 1E13 and 1E17/cm^2.

Regarding claim 26, Koizumi et al. and Kluth et al. together teach the method of claim 1. Koizumi et al. further teaches that the transistor has a second source/drain contact; the implanting further includes implanting the particles into the second source/drain contact region; the activating of the germanium further includes activating the germanium implanted into the second source/drain contact region; and the implanting of the source/drain dopant further includes implanting the source/drain dopant into the second source/drain contact region; further comprising forming a second metal silicide over the second region to form a second contact (Fig. 27B; column 11, lines 34-50).

Koizumi et al. does not teach implanting the germanium at a dose not exceeding 1E17/cm^2, or forming a nickel silicide over the second source/drain contact region after the activating to form the second contact.

Koizumi et al. does teach implanting the germanium at a dose of 4E17/cm^2, and it has been held that "where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller* 105 USPQ233, 255 (CCPA 1955)."

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Koizumi et al. and optimize the conditions to arrive at a germanium implantation dose of not more than 1E17/cm^2.

Kluth et al. teaches a method of forming source/drain contacts including forming a nickel silicide over the source/drain contact region (column 4, lines 36-38).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a semiconductor device according to the method taught by Koizumi et al. and forming a nickel silicide, as taught by Kluth et al. The motivation for doing so at the time of the invention would have been to produce a silicide that forms a first low-resistivity phase at relatively low temperatures (column 2, lines 15-20) to decrease the resistance of the second source/drain contacts.

Regarding claim 36, Koizumi et al. teaches a method of forming a semiconductor device, the method comprising:

- forming a gate over a silicon substrate, the substrate having a lattice having a lattice constant (Fig. 27B);

- increasing the lattice constant of the lattice in a source/drain region of the substrate after the forming the gate by implanting germanium using the gate as a mask (Fig. 27B; column 11, lines 34-50; Si has lattice constant 0.543 nm, Ge has lattice constant 0.566 nm, SiGe has lattice constant between 0.543 and 0.566 nm, depending upon the Ge concentration, see U.S. 5,770,512 to Murakoshi et al.); and
- implanting a source/drain dopant into the source/drain region, wherein the implanting the source/drain dopant is performed subsequent to the increasing the lattice constant (column 11, lines 51-52).

Koizumi et al. does teach implanting the germanium at a dose of 4E17 atoms per centimeter, and it has been held that "where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller* 105 USPQ233, 255 (CCPA 1955)."

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Koizumi et al. and optimize the conditions to arrive at a germanium implantation dose of not more than 1E17/cm^2.

Kluth et al. teaches a method of forming source/drain contacts including forming a nickel silicide over the source/drain contact region (column 4, lines 36-38).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a semiconductor device according to the method taught by Koizumi et al. and forming a nickel silicide, as taught by Kluth et al. The motivation for doing so at the time of the invention would have been to produce a silicide that forms

a first low-resistivity phase at relatively low temperatures (column 2, lines 15-20) to decrease the resistance of the source/drain contacts.

Regarding claim 44, Koizumi et al. teaches a method of forming a semiconductor device, the method comprising:

- forming a gate over a silicon semiconductor substrate (Fig. 27B);
- implanting particles including germanium into a region of the substrate after the forming the gate using the gate as a mask (Fig. 27B; column 11, lines 34-50);
- activating the germanium implanted into the region (column 11, lines 34-50); and
- implanting a source/drain dopant into the substrate for forming at least a portion of a source/drain region in the substrate, wherein the implanting the source/drain dopant is performed subsequent to the activating the germanium (column 11, lines 51-52).

Koizumi et al. does not teach implanting the germanium at a dose not exceeding 1E17/cm^2, or forming a nickel silicide over the source/drain contact region after the activating to form the contact.

Koizumi et al. does teach implanting the germanium at a dose of 4E17 atoms per centimeter, and it has been held that "where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller* 105 USPQ233, 255 (CCPA 1955)."

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Koizumi et al. and optimize the conditions to arrive at a germanium implantation dose of not more than 1E17/cm^2.

Kluth et al. teaches a method of forming source/drain contacts including forming a nickel silicide over the source/drain contact region (column 4, lines 36-38).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a semiconductor device according to the method taught by Koizumi et al. and forming a nickel silicide, as taught by Kluth et al. The motivation for doing so at the time of the invention would have been to produce a silicide that forms a first low-resistivity phase at relatively low temperatures (column 2, lines 15-20) to decrease the resistance of the source/drain contacts.

Regarding claim 45, Koizumi et al. teaches in a transistor device structure having a gate stack (Fig. 27B) and source/drain contact regions comprised primarily of a first material, wherein the source/drain contact regions have a lattice constant, a method of forming a contact, comprising:

- implanting germanium into the source/drain contact regions using the gate stack as a mask (column 11, lines 34-50); and
- activating the germanium implanted into the source/drain contact regions to increase the lattice constant of the source/drain contact regions (column 11, lines 34-50; Si has lattice constant 0.543 nm, Ge has lattice constant 0.566 nm, SiGe has lattice constant between 0.543 and 0.566 nm,

depending upon the Ge concentration, see U.S. 5,770,512 to Murakoshi et al.)

Koizumi et al. does not teach implanting the germanium at a dose not exceeding 1E17/cm^2, or forming a nickel silicide over the source/drain contact region after the activating to form the contact.

Koizumi et al. does teach implanting the germanium at a dose of 4E17 atoms per centimeter, and it has been held that "where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller* 105 USPQ233, 255 (CCPA 1955)."

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Koizumi et al. and optimize the conditions to arrive at a germanium implantation dose of not more than 1E17/cm^2.

Kluth et al. teaches a method of forming source/drain contacts including forming a nickel silicide over the source/drain contact region (column 4, lines 36-38).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a semiconductor device according to the method taught by Koizumi et al. and forming a nickel silicide, as taught by Kluth et al. The motivation for doing so at the time of the invention would have been to produce a silicide that forms a first low-resistivity phase at relatively low temperatures (column 2, lines 15-20) to decrease the resistance of the source/drain contacts.

Claims 8, 14, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi et al. (U.S. 5,475,244) in view of Kluth et al. (U.S. 6,486,062), as applied to claims 1 and 19 above, and further in view of Erokhin et al. (U.S. 2003/0087504).

Regarding claims 8, 14, and 25, Koizumi et al. and Kluth et al. together teach the method of claims 1 and 19 (note 35 U.S.C. 103(a) rejection above), but do not teach that the activating includes heating the source/drain contact region to a temperature greater than 1000 °C—as further limited by claim 8—or implanting the particles is performed at a temperature between 25 and 600 °C—as further limited by claims 14 and 25.

Erokhin et al. teaches a method of implanting germanium into silicon at a temperature between 25 and 600 °C (paragraphs 0011-0012) and subsequently annealing at a temperature greater than 1000 °C (paragraph 0048).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Koizumi et al. and Kluth et al. together and Erokhin et al. by forming contact to a source/drain region of a transistor using the method of claim 1, as taught by Koizumi et al. and Kluth et al. together, by implanting germanium at a temperature between 25 and 600 °C and annealing the germanium implant at a temperature of 1100°C, as taught by Erokhin et al., since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art (*In re Aller*, 105 USPQ 233 (CCPA 1955)).

Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi et al. (U.S. 5,475,244) in view of Kluth et al. (U.S. 6,486,062), as applied to claim 1 above, and further in view of Downey (U.S. 2002/0187614).

Regarding claims 10 and 11, Koizumi et al. and Kluth et al. together teach the method of claim 1 (note 35 U.S.C. 103(a) rejection above), but do not teach that the activating further includes rapid thermal annealing or laser annealing of the source/drain contact regions.

Downey teaches a method of implanting silicon with germanium and activating the germanium by rapid thermal annealing and laser annealing (paragraph 0032).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Koizumi et al. and Kluth et al. together and Downey by forming a contact to a source/drain contact region of a transistor device using the method of claim 1, as taught by Koizumi et al. and Kluth et al. together, by activating the germanium implant by rapid thermal annealing or laser annealing, as taught by Downey. The motivation for doing so at the time of the invention would have been to cause chemical bonding between the substrate and the implanted material, as taught by Downey (paragraph 0031).

Claims 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi et al. (U.S. 5,475,244) in view of Kluth et al. (U.S. 6,486,062) and Downey (U.S. 2002/0187614).

Regarding claims 34 and 35, Koizumi et al. teaches a method of forming a semiconductor device, the method comprising:

- providing a silicon substrate (**2740** in Fig. 27A);
- forming a gate over the silicon substrate (**2744/2745** in Fig. 27B);
- implanting germanium into a region of the silicon substrate using the gate as a mask (Fig. 27B; column 11, lines 34-50); and
- activating the germanium implanted into the region of the substrate.

Koizumi et al. does not teach that implanting germanium at a dose not exceeding $1E17/cm^2$, that the germanium implant activation is performed with a non-diffusion activation process, or forming a nickel silicide over the region after the activating.

Koizumi et al. does teach implanting the germanium at a dose of $4E17/cm^2$, and it has been held that "where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller* 105 USPQ233, 255 (CCPA 1955)."

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Koizumi et al. and optimize the conditions to arrive at a germanium implantation dose of not more than $1E17/cm^2$.

Downey teaches a method of implanting silicon with germanium and activating the germanium by rapid thermal annealing and laser annealing, non-diffusion activation processes (paragraph 0032).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Koizumi et al. and Kluth et al. together and Downey by forming a contact to a source/drain contact region of a transistor device, as taught by Koizumi et al. and Kluth et al. together, by activating the

germanium implant by rapid thermal annealing or laser annealing, as taught by Downey. The motivation for doing so at the time of the invention would have been to cause chemical bonding between the substrate and the implanted material, as taught by Downey (paragraph 0031).

Kluth et al. teaches a method of forming source/drain contacts including forming a nickel silicide over the source/drain contact region (column 4, lines 36-38).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a semiconductor device according to the method taught by Koizumi et al. and forming a nickel silicide, as taught by Kluth et al. The motivation for doing so at the time of the invention would have been to produce a silicide that forms a first low-resistivity phase at relatively low temperatures (column 2, lines 15-20) to decrease the resistance of the source/drain contacts.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi et al. (U.S. 5,475,244) in view of Kluth et al. (U.S. 6,486,062), as applied to claim 1 above, in view of Imai (U.S. 5,506,427).

Regarding claim 12, Koizumi et al. and Kluth et al. together teach the method of claim 1 (note 35 U.S.C. 103(a) rejection above), but do not teach that the activating further includes arc lamp thermal annealing of the source/drain contact region.

Imai teaches a method of annealing SiGe by arc lamp annealing (column 6, lines 7-10).

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Koizumi et al. and Kluth et al.

together and Imai by forming a contact to a source/drain contact region of a transistor device using the method of claim 1, as taught by Koizumi et al. and Kluth et al. together, by activating the germanium implant by laser arc annealing, as taught by Imai. The motivation for doing so at the time of the invention would have been to avoid degrading transistor characteristics, as expressly taught by Imai (column 5, line 66 – column 6, line 2).

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi et al. (U.S. 5,475,244) in view of Kluth et al. (U.S. 6,486,062), as applied to claim 1 above, and further in view of Murakoshi et al. (U.S. 5,770,512).

Regarding claim 13, Koizumi et al. and Kluth et al. together teach the method of claim 1 (note 35 U.S.C. 103(a) rejection above), but do not teach that the activating includes gas convection annealing of the source/drain contact region.

Murakoshi et al. teaches a method of activating germanium ion-implanted into silicon by convectively heating it in a nitrogen gas atmosphere at 550°C for an hour to recrystallize the silicon wafer following ion implantation (column 14, lines 44-52).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a contact to a source/drain contact region according to the method of claim 1 as taught by Koizumi et al. and Kluth et al. together, and use gas convection annealing to activate the germanium implantation, as taught by Murakoshi et al. The motivation for doing so at the time of the invention would have been to recrystallize the silicon wafer following ion implantation, as noted above and taught by Murakoshi et al.

Claims 17, 18, 20, 28, 30, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi et al. (U.S. 5,475,244) in view of Kluth et al. (U.S. 6,486,062), as applied to claims 1 and 19 above, and further in view of Chakravarthi et al. (U.S. 6,797,593).

Regarding claims 17 and 18, Koizumi et al. and Kluth et al. together teach the method of claim 1 (note 35 U.S.C. 103(a) rejection above), but do not teach forming a sidewall spacer adjacent to a sidewall of the gate, wherein the implanting the germanium is performed prior to the forming the sidewall spacer and wherein the forming the sidewall spacer is performed prior to the implanting the source/drain dopant.

Chakravarthi et al. teaches a method for forming a MOSFET drain extension activation, including forming a sidewall spacer adjacent to the sidewall of the gate and implanting arsenic into drain extension regions, wherein the implanting the arsenic (**314** in Fig. 4A) is performed prior to the forming the sidewall spacer (**318** in Fig. 4A; column 2, lines 25-38) and wherein the forming the sidewall spacer is performed prior to the implanting the source/drain dopant (**320** in Fig. 4A).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a contact to a source/drain contact region of a transistor device using the method of claim 1, as taught by Koizumi et al. and Kluth et al. together, and further form a sidewall spacer adjacent to a sidewall of the gate, wherein the implanting the germanium is performed prior to the forming the sidewall spacer, and wherein the forming the sidewall spacer is performed prior to the implanting the source/drain dopant, as taught by Chakravarthi et al. The motivation for doing so at the

time of the invention would have been to use the sidewall spacers to mask the implantation of the source/drain dopant, as taught by Chakravarthi et al. (column 3, line 65 – column 4, line 3), after the particle implantation.

Regarding claim 20, Koizumi et al. and Kluth et al. together teach the method of claim 19 (note 35 U.S.C. 103(a) rejection above) but do not teach implanting a second source/drain dopant in the semiconductor substrate after the implanting the source/drain dopant, wherein the second source/drain dopant is implanted deeper than the source/drain dopant.

Chakravarthi et al. teaches implanting a second source/drain dopant (**320** in Fig. 4A;) in the semiconductor substrate after the implanting the source/drain dopant (drain extensions, **314** in Fig. 4A), wherein the second source/drain dopant is implanted deeper than the source/drain dopant (see Fig. 3, which shows that the extension implants are less deep than the subsequent source/drain dopant implants).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a contact to a source/drain contact region by using the methods of claims 1 and 19, as taught by Koizumi et al. and Kluth et al. together, and further implant a second source/drain dopant in the semiconductor substrate after the implanting the source/drain dopant, wherein the second source/drain dopant is implanted deeper than the source/drain dopant, as taught by Chakravarthi et al. The motivation for doing so at the time of the invention would have been to form drain extensions and thereby combat channel hot carrier effects, as taught by Chakravarthi et al. (column 2, line 11).

Regarding claim 28, Koizumi et al. and Kluth et al. together teach the method of claim 1 (note 35 U.S.C. 103(a) rejection above), wherein the gate is over a semiconductor substrate and a channel is in the substrate under the gate, but does not teach forming a source/drain extension adjacent to the channel in the semiconductor substrate.

Chakravarthi et al. teaches forming a source/drain extension adjacent to the channel in the semiconductor substrate (column 2, lines 25-26) to combat channel hot carrier effects (column 2, line 11).

Therefore, at the time of the invention, it would have been obvious to form a contact to a drain/source contact region using the method according to claim 1 and as taught by Koizumi et al. and Kluth et al. together, and further form a source/drain extension adjacent to the channel in the semiconductor substrate, as taught by Chakravarthi et al., to combat channel hot carrier effects, as noted above as expressly taught by Chakravarthi et al.

Regarding claim 30, Koizumi et al. and Kluth et al. and Chakravarthi et al. together teach the method of claim 28 (note 35 U.S.C. 103(a) rejection above). Chakravarthi et al. further teaches implanting a second source/drain dopant into the substrate for forming the source/drain extension (**314** in Fig. 4A), wherein the implanting the second source/drain dopant is performed prior to the implanting the source/drain dopant (**320** in Fig. 4A).

Regarding claim 31, Koizumi et al. and Kluth et al. together teach the method of claim 1 (note 35 U.S.C. 103(a) rejection above), but do not teach further activating the source/drain dopant.

Chakravarthi et al. teaches activating the source/drain dopant (**322** in Fig. 4A) to diffuse implanted dopants to a final drain extension junction depth (column 12, lines 6).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a contact to a source/drain contact region according to the method of claim 1, as taught by Koizumi et al. and Kluth et al. together, and further activate the source/drain dopant, as taught by Chakravarthi et al., to cause the dopants to diffuse to a desired drain extension junction depth.

Claims 22, 27, 42, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi et al. (U.S. 5,475,244) in view of Kluth et al. (U.S. 6,486,062) as applied to claims 1, 19, 36, and 45 above, and further in view of Aronowitz et al. (U.S. 5,296,387).

Regarding claim 22, Koizumi et al. and Kluth et al. together teach the method of claim 1, but do not teach that the implanting the germanium includes implanting with an energy in the range of 3 KeV to 50 KeV.

Aronowitz et al. teaches implanting germanium into the source and drain regions of a transistor with an energy in the range of 3 KeV to 50 KeV (column 2, lines 32-36).

Therefore, at the time of the invention, it would have been obvious for one of ordinary skill in the art to use the method taught by Koizumi et al. and Kluth et al. together, and further implant the germanium at an energy level in the range of 3KeV to

50 KeV, as taught by Aronowitz et al. to be effective for germanium-doping source/drain regions of silicon substrates.

Regarding claims 27, 42, and 46, Koizumi et al. and Kluth et al. together teach the method of claims 1, 36, and 45 (note 35 U.S.C. 103(a) rejection above). They do not teach that the source/drain dopant includes boron—further limited by claims 27 and 42—or a p-type material—further limited by claim 46.

Aronowitz et al. teaches implanting germanium into the source and drain regions of a transistor, activating the germanium implants, doping the source/drain contact regions with boron, a p-type material (column 3, lines 60-64), and then forming a metal silicide (column 4, lines 52-68).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Koizumi et al. and Kluth et al. together, and further use boron (p-type material) as the source/drain implant, since Aronowitz et al. teaches that either n- or p-type materials are appropriate for use in a transistor with germanium-implanted source/drain contact regions.

Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi et al. (U.S. 5,475,244) in view of Kluth et al. (U.S. 6,486,062) and Aronowitz et al. (U.S. 5,296,387) as applied to claim 42 above, and further in view of Xiang (U.S. 2005/0054164).

Regarding claim 43, Koizumi et al, Kluth et al., and Aronowitz et al. together teach the method of claim 42 (note 35 U.S.C. 103(a) rejection above). They do not

teach that the source/drain dopant includes a source/drain extension dopant for forming a source/drain extension in the substrate.

Xiang teaches that the use of shallow source and drain extensions in MOSFETs reduce short-channel effects, which is particularly important as MOSFET dimensions are reduced (paragraph 0007).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Koizumi et al., Kluth et al., and Aronowitz et al., and further use the source/drain dopant to create source/drain extensions, since Xiang teaches that source/drain extensions reduce short-channel effects in MOSFETs.

Response to Arguments

Applicant's arguments with respect to claims 1-3, 7-14, 17-28, 34-36, and 42-46 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hwang et al. (U.S. 6,911,706) teaches using a gate to mask a germanium implantation of a source/drain contact region, followed by source/drain extension implantation and rapid thermal processing.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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